In the claims:

1-19 (canceled)

20. (previously presented) An integrated circuit, comprising:

a first dielectric layer disposed outwardly from a substrate;

a plurality of gate stacks, each gate stack comprising:

a floating gate body disposed outwardly from the first dielectric layer;

a second dielectric region disposed outwardly from the floating gate body; and

a first polysilicon layer disposed outwardly from the second dielectric region;

a plurality of dielectric isolation regions disposed between the gate stacks, the dielectric isolation regions formed after the formation of the gate stacks;

a second. polysilicon layer disposed outwardly from the first polysilicon layer and the dielectric isolation regions;

a peripheral dielectric layer disposed outwardly from the second polysilicon layer and a peripheral region of the substrate, the peripheral region of the substrate disposed adjacent to a region of the substrate supporting the gate stacks;

at least one peripheral gate body disposed outwardly from the peripheral region of the substrate.